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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SAXENA, AKASH	

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/673,583
Filing Date: September 30, 2003
Appellant(s): MITROVIC, ANDREJ S.

Steven P. Weihrouch
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/17/2008 appealing from the Final Office action mailed 06/02/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

10/673,467; 10/673,501; 10/673,506; 10/673,507 and 10/673,138.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

- 35 USC 112 1st Paragraph Rejection of Claims 1-40 and 44-46.
- Double Patenting rejection against applications 10673501 and 10673583.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(**8) Evidence Relied Upon**

- **USPAT 6,802,045 Sonderman et al**
- **"Mathematic-Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena"; V.K.Jain et al; IEEE 1994**
- **USPAT 5,719,796 Chen et al**

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(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. **Claims 1-11, 13-14, 17-19, 21-27, 28-32, 33-38, 40-41, 44-46, 48-54 and 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).**

Regarding Claim 1

Sonderman teaches a method to facilitate a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting process data relating to the actual process performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; Col.7 Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool describing at least one of a basic physical or chemical attributes (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation for the actual process being performed during performance of actual process (Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63; Fig. 1-3) using the input data and the physical model to provide virtual sensor measurements relating to the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the virtual sensor measurements obtained during the performance of the actual

process (Sonderman: Fig. 1-3 Col.7 Lines 4-7; Col.3 Lines 56-63) to facilitate the actual process being performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.7 Lines 37-65).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

Jain also teaches said first principles simulation (MPE Engine) result being produced in a time frame shorter in time than the actual process being performed as MPE engine solving the problem in real time (Jain: Abstract), with further speed-up possible by distributed simulation and enhancement in wafer technology (Jain: Fig.4 & 5 and sections IV and V).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; Col.7 Lines 8-20).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the process data relating to the actual process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claim 11

Sonderman teaches repeating the step of inputting the data from (physical sensor) metrology tool into first principle simulation and facilitating the semiconductor process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process (Sonderman: at least in Col.4 Lines 48-Col.5 Lines 10; Col.7 Lines 36-53; col.4-7).

Regarding Claims 13-14

Sonderman teaches performing first principle simulation not concurrently with the process performed; inputting data from at least one initial condition recorded from a previous process performed (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 17

Sonderman teaches using virtual sensor measurements to characterize the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 11-17; equipment model).

Regarding Claim 18

Sonderman teaches using virtual tool measurements to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 41-47).

Regarding Claim 19

Sonderman teaches using virtual sensor measurements to detect a fault in the process performed by the semiconductor-processing tool (Sonderman teaches: at least in Col.7, Fig 5-6).

Regarding Claims 21-25

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65) to perform first principle simulation *(Jain: Section III)* recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 26-27

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 28

System claim 28 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 29

System claim 29 discloses substantially similar limitations as method claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 30-32

System claims 30-32 disclose substantially similar limitations as method claims 3-5 and are rejected for the same reasons as claims 3-5.

Regarding Claims 33-36

System claims 33-36 disclose substantially similar limitations as method claims 6-9 and are rejected for the same reasons as claims 6-9.

Regarding Claim 37

System claim 37 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 38

System claim 38 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claims 40-41 and 61

System claims 40-41 and 61 disclose substantially similar limitations as method claims 13-14 and are rejected for the same reasons as claims 13-14.

Regarding Claim 44

System claim 44 discloses substantially similar limitations as method claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 45

System claim 45 discloses substantially similar limitations as method claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 46

System claim 46 discloses substantially similar limitations as method claim 19 and is rejected for the same reasons as claim 19.

Regarding Claims 48-52

System claims 48-52 disclose substantially similar limitations as method claims 21-25 and are rejected for the same reasons as claims 21-25.

Regarding Claims 53-54

System claims 53-54 disclose substantially similar limitations as method claims 26-27 and are rejected for the same reasons as claims 26-27. Dependency of claim 53 is changed from 48 to 28 and is noted by examiner.

Regarding Claim 62

System claim 62 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 63-64

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section

"Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

2. Claims 12, 15-16, 20, 39, 42-43, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).

Regarding Claim 12

Teachings of Sonderman & Jain are disclosed in claim 1 rejection above. Sonderman teaches setting boundary condition for first principle simulation through the process parameters (Sonderman: at least in Col.5-6).

Sonderman & Jain do not teach performing time dependent concurrent simulation without direct input from semiconductor process to facilitate semiconductor process based on virtual sensor measurement.

Chen teaches time dependent concurrent simulation without direct input from semiconductor process and applies the result to facilitate the semiconductor process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process. Chen teaches simulation based on the statistical data, which in turn provides the output to actual fabrication process (Chen: at least in Col.3 Lines 12-18).

Motivation to combine Jain to Sonderman is provided above in claim 1 rejection.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23). Chen facilitates in building the process model that can be run in parallel to actual process thereby providing more specific embodiment to Sonderman's teachings (Chen: Col.3 Lines 12-24).

Regarding Claim 15

Chen teaches indirectly putting best-known input parameters for the physical model (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 16

Chen teaches comparing virtual sensor measurements with the actual sensor measurements and refining at least one best known input parameters and the physical model to obtain better agreement between the virtual sensor measurements with actual sensor measurements (Chen: at least in Col.3 Lines 48-57; Calibrate run calibrate simulated).

Regarding Claim 20

Chen teaches storing virtual sensor measurement in a library for subsequent use in a first principle simulation (Chen: at least in Col.3; Specifically in Col.3 Lines 37-41).

<u>Regarding Claim 39</u>

System claim 39 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

<u>Regarding Claim 42</u>

System claim 42 discloses substantially similar limitations as method claim 15 and is rejected for the same reasons as claim 15.

<u>Regarding Claim 43</u>

System claim 43 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

<u>Regarding Claim 47</u>

System claim 47 discloses substantially similar limitations as method claim 20 and is rejected for the same reasons as claim 20.

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(10) Response to Argument

A. Regarding the 35 USC 112 1st Paragraph Rejection of Claims 1-54 and 62-64

Although examiner has withdrawn the rejection under this statue, and the claims are given the broadest reasonable interpretation consistent with the specification, the arguments provided for claim 1 and 23 limitations are more specific than the limitations. Specifically, the limitation

> "… performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, **said first principles simulation result being produced in a time frame shorter in time than the actual process being performed**, and"

as argued by the appellant on Pg.13 of appeal brief, states reasons *why the time frame is shorter*, are more specific than claimed above. Further as shown by Fig.3 on same page the simulation module 302 is not claimed to be the part of the tool 102.

B. Regarding the 35 USC 103 Rejection of Claims 1-54 and 62-64 over Sonderman et al and Jain et al

(Argument 1) Appellant has argued in Remarks Pg.16:

> The plain reading of this section of Sonderman et al is that the system 100 then (e.g., at time T 1) optimizes the simulation for each silicon wafer, Si to be processed (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer ***to be processed***. Thus, Appellant respectfully submits that Sonderman et al teach performing a simulation result for a process to be performed before performance of the actual process, and do **not** teach the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.

(Response 1) Appellant above cites Sonderman Col.9 Lines 45-61 Stating:

> FIG. **10** illustrates a chart that represents the percentage effectiveness of the each process performed on each silicon wafer (S_1, S_2 . . . S_i). Some processes P_i can be more effective than others in reaching a desired performance goal. The electrical parameter Y, relating to the processed silicon wafer S_i, is generally a multi-variant function of S_i process steps, as illustrated by Equation 2.
>
> $$Y=f(S_1, S_2, S_3 \ldots S_i) \qquad \text{Equation 2}$$
>
> The system **100** then optimizes the simulation (described above) to find more optimal process target (T_i) for each silicon wafer, S_i to be processed. These target values are then used to generate new control inputs, X_{Ti}, on the line **805** to control a subsequent process of a silicon wafer S_i. The new control inputs, X_{Ti}, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool **120** operating scenarios, and the like.

Here examiner would like to emphasize that new control inputs X_{Ti} are generated to control the "subsequent [part of the] process" (applicable to same process as inputs are *pertinent* to same process only - e.g. metal deposition on substrate where inputs may specify to deposit more metal) on the silicon wafer $\underline{S_i}$.

Arguendo, If Sonderman was intending to use the inputs for the next wafer he would have stated for silicon wafer $\underline{S_{i+1}}$, with emphasis on subscript i+1.Therefore as the limitation "***for the actual process being performed during performance of the actual process***", is performed during the processing of silicon wafer (See Sonderman Fig.1).

(Argument 2) Appellant has argued in Remarks Pg.16-18:

> “Other sections of Sonderman et al support Appellant's position on this matter that the **simulation results in Sonderman et al are made prior to controlling a subsequent process**. For instance, Figure 4 of Sonderman et al (reproduced below) shows that the simulation results are produced ahead of performing a process and **thus have to be based on historical data**.
>
> … With reference to **Figure 4, Sonderman et al disclose at col. 6, lines 24-47**:…
>
> Appellant respectfully points out that this description in Sonderman et al is a description of a **feedback loop** as Sonderman et al describe just below that portion which the examiner emphasized. **Feedback** modification is by definition the control of future wafers based on what has already occurred to a previous wafer. Hence, this section supports rather than refutes Appellant's position on this matter.”

(Response 2) Examiner respectfully disagrees as Sonderman Col.4 Lines 65-Col.5 Lines 10 states:

> Furthermore, the simulation environment **210** can be used for feedback modification of control parameters invoked by the process control environment **180**. For example, the

> **5**
>
> manufacturing environment **170** can send metrology data results into the simulation environment **210**. The simulation environment **210** can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment **180**. A feedback loop in then completed when the process control environment **180** sends the modified or adjusted process control parameters to the manufacturing environment **170** for further processing of semiconductor wafers.

As clearly seen, the control parameter from the process control environment are first fed into the simulation environment, and then the post simulation output, having modified control parameters, is used to control the process control environment. Thus the results are not based on the historical data for another run, but are from the same run, where the input from *the* process control environment provided to

simulation tool is used to generate modified control parameter for <u>*the*</u> process control environment.

Appellant recital of Sonderman Col.6 and Fig.4 are noted, however they are part of the picture shown in the Col.4 teaching above of the Sonderman. Appellant is picking in the chicken & egg situation, which one came first. As stated the process control is a feedback process (See Sonderman Fig.1 and 8) where the metrology data is used as input to simulation tool (Fig.1) and output as shown above is applied to subsequent part of the process.

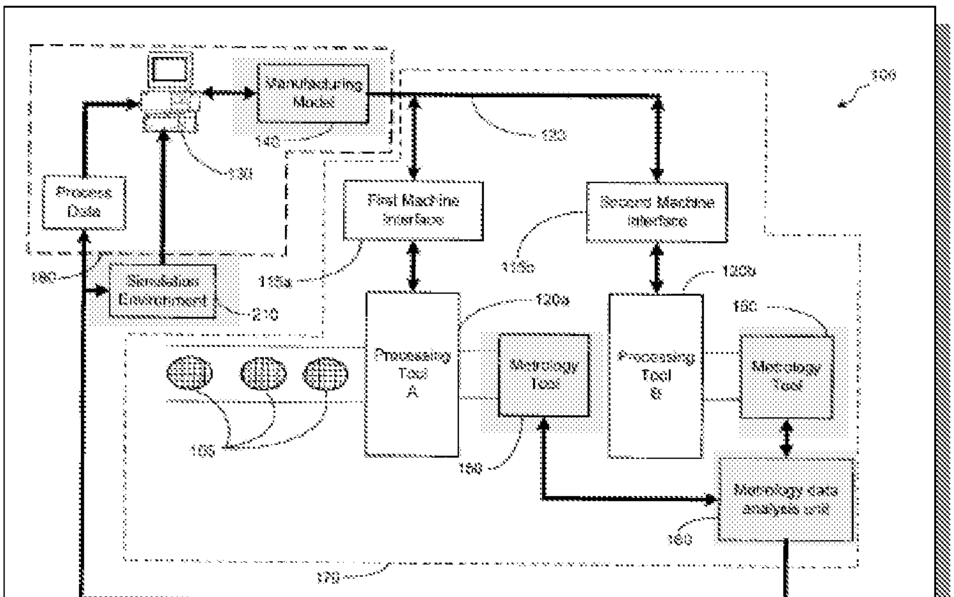

FIGURE 1

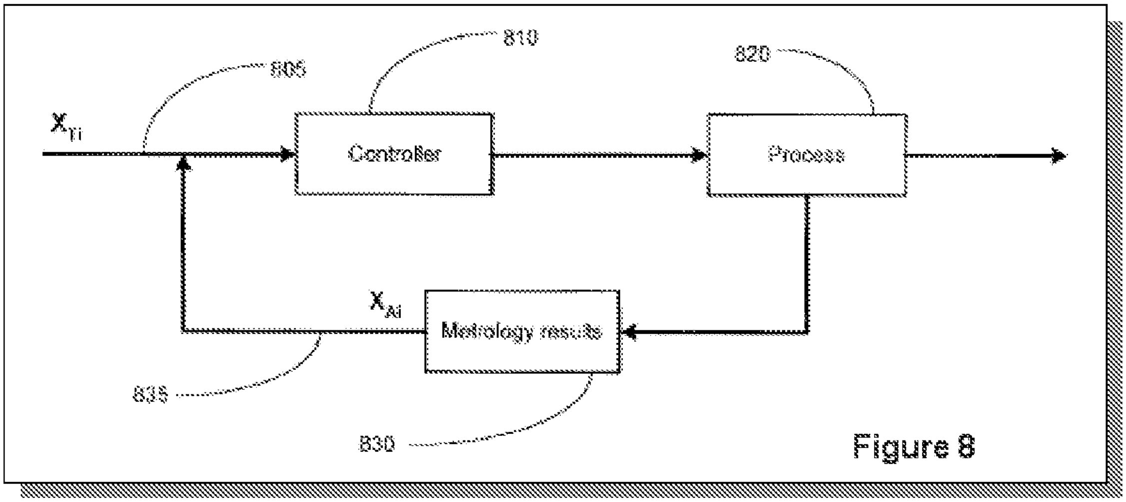

Figure 8

(Argument 3) Appellant has argued in Remarks Pg.18:

> Accordingly, Appellant respectfully submits that Sonderman et al do not disclose and indeed ***teach away*** from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, **[1]** which is produced for the actual process being performed during performance of the actual process for control of the actual process. **[2]**

(Response 3) Appellant has not presented any rationale why Sonderman teaches away. As shown argument [1] is taught by Sonderman in Col.4 Line 65-Col.5 Line 10. As shown above argument [2] is taught by Sonderman in Col.9 Lines 40-51 (See response 1).

(Argument 4) Appellant has argued in Remarks Pg.19:

> The deficiencies in Sonderman et al are not overcome by Jain et al. The Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Jain et al for their teaching of computer encoded differential equations in a mathematical physical engine (MPE) which can be applied to wafer processing. See Office Action, page 16. Jain et al describe at pages 372-373 that:…
> Thus, as emphasized above, the proposed development work in Jain requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.

(Response 4) Teaching of Jain, in defining the MPE as first principle simulation model, are adequate in terms of modeling the semiconductor environment. Further, appellants own specification does not disclose any more details than present in Jain. (Please see Specification [0035]-[0036]).

(Argument 5) Appellant has argued in Remarks Pg.20-23:

> Arguments pertaining to Tan and Kee references.

(Response 5) Although, Tan and Kee references are not presented as grounds of rejection in this case and arguments pertaining to them are not relevant to instant rejection, Examiner notes reference being made to APC control (In Tan), which is also present in Sonderman. It is common knowledge in the art of semiconductor processing that Advanced Process Control (APC) is a real-time system which provides process control to semiconductor processing tool. As seen from Sonderman APC control integrates the simulation tool (Sonderman: Col.9 Lines 57-Col.10 Line 20) therefore by sheer nature, the simulation tool also need to be real time and *not run sequentially* as suggested by appellant in previous arguments. Sonderman does not suggest any historical database as suggested in Tan.

(Argument 6) Appellant has argued in Remarks Pg.23:

> The examiner in the final Office Action did not apply but rather noted the IEEE 1990 paper by Su-shing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring," hereinafter referred to as AEMPS, as evidence that the newly added limitation (said first principles simulation result being produced in a time frame shorter in time than the actual process being performed) is known in the art. Yet, AEMPS describes the use of simulation in neural network environment used to "leam processes and the equipment model." See page 120, section 4. AEMPS describes in section 4 that "a rule-based expert system provides human interfaces and high-level decision support." Accordingly, AEMPS does not describe a first principles simulation result, but rather describes a neural network leaming-based simulation…

(Response 6) First AEMPES was not used in the rejection. Secondly, even if used appellant is performing piecemeal analysis of AEMPES as the first simulation model is taught by Jain. Arguments pertaining to AEMPES are withdrawn and not applicable to instant invention.

(Argument 7) Appellant has argued in Remarks Pg.24-25:

> More importantly, numbered paragraphs [0004] and [005] indicate at most that the times for a large number of simulations typically done in the tool design stage are comparable to wafer or wafer cassette processing times. <u>There is no statement here regarding how long the times would be for a process control simulation.</u> Further, numbered paragraphs [0004] and [005] indicate that, at the time of the invention, there were serious impediments which would mean that it would not be possible, prior to the invention, to produce a first

(Response 7) As seen from the cited paragraphs [0004]:

> "…Indeed, the present inventors have recognized that a large number of simulations typically done in the tool design stage can presently be <u>**run in times comparable to wafer or wafer cassette processing times**</u>…"

Clearly refers to the time period of the simulation as comparable to the wafer processing times. Therefore the statement [1] above is contradictory to what specification background states.

(Argument 8) Appellant has argued in Remarks Pg.25:

> Hence, Tan et al, Jain et al, Kee et al, AEMPES, and the background section of the specification all <u>discredit any suggestion that the examiner may have read from the disclosure of Sonderman et al for real-time simulation and control of an actual process being performed</u>.

(Response 8) Besides being conclusory, the statement above contradicts what is known in the art as real time control - i.e. Advanced Process Control (APC) for the semiconductor processing tools. Sonderman (Col.9 Lines 57-Col.10 Line 20) clearly shows integration of the simulation tool with APC and by definition APC is real time, it implies real time simulation as well. Further Appellant has never claimed "real-time

simulation and control" as argued against Sonderman & Jain and implied from Tan et al, Jain et al, Kee et al, & AEMPES.

(Argument 9) Appellant has argued in Remarks Pg.26:

> In the present situation, the claimed elements worked together in an unexpected and fruitful manner as compared to the prior art. For example, since in Sonderman et al there are new control inputs for each subsequent wafer, **[1]** one can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the historically lengthy time for generation of a first principles model simulation would mean that, in Sonderman et al, one is prevented from realizing a real time process control based on a first principles simulation during the actual process being performed. **[2]** Meanwhile, the claimed processes and systems (by producing a first principles simulation result in a time frame shorter in time than the actual process being performed) permits accurate control of the process even if the system being controlled deviates from its historical behavior.

(Response 9) As per [1], this allegation is unsubstantiated and rebutted above in Response 1. As per [2], appellant is reading deficiencies presented in older reference Tan (dated 2001) and Kee (dated 1996) into more current Sonderman (dated 2004) without providing support for the allegation in [2] that Sonderman is not able to overcome those deficiencies. Further, it seems appellant is presenting argument against validity and operability of Sonderman's teaching. Under 35 USC 282, a patent is presumed valid for it teachings.

C. Regarding the 35 USC 103 Rejection of Claims 63 and 64 over Sonderman et al and Jain et al

(Argument 10) Appellant has argued in Remarks Pg.26-27:

> Claim 63 defines that the performing a first principles simulation includes providing for the first principles simulation a reuse of known solutions as initial conditions for the first principles simulation. The Office Action notes that "Jain teaches use of Navier Stokes and other known simulation solutions" and cites pp. 367-368 of Jain et al. However, the Navier Stokes equation on page 367 of Jain et al is a fluid flow equation which needs boundary conditions and which need s to be solved in order to produce a solution. The Navier Stokes equation on page 367 of Jain et al does not represent a solution, much less the reuse of known solutions as initial conditions for the first principles simulation. Appellant's inspection of the remainder of Jain et al finds no disclosure of the reuse of known solutions as initial conditions for the first principles simulation.

(Response 10) Jain presents the model used in the assertion of initial condition would be obvious to one skilled in the art of using the model to initialize the model. For example, also see Sonderman (Col.7 Lines 8-20) teaches initializing. Appellant appears to be performing piecemeal analysis.

D. Regarding the Double Patenting Rejections

Double patenting rejection is withdrawn in view of the terminal disclaimer filed by appellant.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Akash Saxena/

Examiner, Art Unit 2128

Conferees:

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123